REMARKS

Claims 1 and 3-23 are pending in this application. The May 26, 2004 Office Action allowed Claims 1, 3-20, 22 and 23, and rejected Claim 21 under 35 U.S.C. 103(a). The foregoing amendment amends Claims 12 and 15 to correct certain typographical errors.

Jaeger and *Takahashi* Do Not Show or Suggest Claim 21

The Examiner rejected Claim 21 as unpatentable over U.S. Patent No. 5,148,383 to Jaeger ("*Jaeger*") in view of U.S. Patent No. 5,809,039 to Takahashi et al. ("*Takahashi*"). The Applicants traverse this rejection for the reasons discussed below.

The precoding of the present invention feeds back a one bit delayed signal obtained from the EXOR output to one input of the same EXOR. The invention differs from the conventional precoder shown in Fig. 1 of the present specification by providing the feedback to the EXOR output within a short time, namely one bit.

In the prior art, a one bit delay is realized by connecting a D-type flip-flop (D-F/F) to the EXOR output as shown in Fig. 3 of the present specification, which is similar to the configuration disclosed in *Jaeger*. This configuration has an advantage that the delay time can be optimized by controlling the phase of the clock inputted into the D-F/F by using the phase shifter, which in turn controls the output timing from the D-F/F. However, a disadvantage of this conventional configuration is that the delay time cannot be shortened.

As shown in Fig. 16 of the present invention, the basic operation of the D-F/F has two steps, one for reading data after the rising edge of the clock signal (at which the Master Latch output is changed) and one for changing the D-F/F output at the falling edge of the clock signal (at which the Slave Latch output is changed). The delay time d2 of the D-F/F contains a delay corresponding to 1/2 of the clock period, which poses a problem in realizing the one bit delay.

As shown in Fig. 4 of the present invention, if the delay time (the sum of d1 and d2) exceeds one bit, a phase shift between the input data at the EXOR input terminal and the fed back data occurs, which causes a notch in the output which in turn can cause the erroneous

operation. Thus, while the conventional configuration has the advantage that the delay time can be controlled by the clock phase, it is difficult to realize for ultra high speed operation because of its large delay.

In order to resolve this problem, the differential encoder of Claim 21 uses a configuration as shown in Fig. 15 (third embodiment) in which the Master Latch output is fed to the slave latch and back to the EXOR input. Although *Takahashi* generally discloses utilizing a Master Latch output, it does not teach or suggest using the Master Latch output for the purpose of shortening the delay time or feeding the Master Latch output to the input side of the EXOR and the slave latch. Thus, neither *Jaeger* nor *Takahashi* discloses a differential encoder which can realize the one bit delay using the D-F/F, while shortening the delay time of the D-F/F, as recited by Claim 21. Accordingly, Claim 21 should be allowed.

CONCLUSION

The foregoing is submitted as a complete response to the Office Action identified above. This application should now be in condition for allowance, and the Applicants solicit a notice to that effect. If there are any issues that can be addressed via telephone, the Examiner is asked to contact the undersigned at 404.685.6799.

Respectfully submitted,

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